

Appl. No.: 10/090,289
Amtd. Dated July 30, 2004
Reply to Office action of May 3, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): An electronic component, comprising:

at least two wiring boards stacked on top of one another and substantially parallel to one another, at least one of said at least two wiring boards having apertures formed therein, said stacked wiring boards including an uppermost wiring board and an undermost wiring board, at least one of said uppermost wiring board and said undermost wiring board having near-edge electrical contacts without said apertures;

at least two semiconductor chips each mounted on a respective wiring board of said at least two wiring boards and electrically connected to said respective wiring board; and

solder connections mechanically and electrically interconnecting said at least two stacked wiring boards, said soldered connections extending through said apertures in at least one of said at least two stacked wiring boards and over one or more levels of said at least two stacked wiring boards.

Applic. No.: 10/090,289
Amdt. Dated July 30, 2004
Reply to Office action of May 3, 2004

Claim 2 (original): The electronic component according to claim 1, wherein said stacked wiring boards have edge regions and said soldered connections are provided in said edge regions.

Claim 3 (original): The electronic component according to claim 1, wherein said soldered connections are respectively formed by solder balls lying one on top of another and fused together.

Claim 4 (original): The electronic component according to claim 3, wherein said solder balls have a smaller diameter than said apertures.

Claim 5 (original): The electronic component according to claim 1, wherein said wiring boards with said semiconductor chips mounted on them are stacked one on top of another in such a way that a rear side of one of said semiconductor chips faces an underside of a neighboring one of said wiring boards.

Claim 6 (original): The electronic component according to claim 1, wherein said wiring boards have undersides with supporting points, and a respective semiconductor chip of said semiconductor chips has a rear side bearing on one of said undersides.

Applic. No.: 10/090,289
Amtd. Dated July 30, 2004
Reply to Office action of May 3, 2004

Claim 7 (original): The electronic component according to claim 6, wherein said supporting points are plastic buffers disposed centrally on said undersides of said wiring boards.

Claim 8 (original): The electronic component according to claim 7, wherein said plastic buffers contain an elastomer.

Claim 9 (cancelled).

Claim 10 (currently amended): The electronic component according to claim 23 1, wherein said undermost wiring board has contact terminal areas.

Claim 11 (currently amended): The electronic component according to claim 23 1, wherein said undermost wiring board has contact bumps.

Claim 12 (original): The electronic component according to claim 10, wherein said undermost wiring board has solder deposits located on said contact terminal areas.

Claim 13 (currently amended): The electronic component according to claim 9 1, wherein said wiring boards which are not said undermost wiring board or said uppermost wiring board have near-edge electrical contacts with said apertures.

Appl. No.: 10/090,289
Amdt. Dated July 30, 2004
Reply to Office action of May 3, 2004

Claim 14 (currently amended): The electronic component according to claim 9 1, wherein said wiring boards which are not said undermost wiring board or said uppermost wiring board have near-edge electrical contacts without said apertures.

Claim 15 (currently amended): A method for producing an electronic component, which comprises the steps of:

providing at least two stacked wiring boards having apertures formed therein electrical contacts disposed thereon and, the stacked wiring boards including an uppermost wiring board and an undermost wiring board, at least one of the uppermost wiring board and the undermost wiring board having near-edge electrical contacts without the apertures;

mounting at least two semiconductor chips on each mounted on and electrically connected to a respective wiring board of the at least two wiring boards and electrically connecting to the respective wiring boards, and at least one of the wiring boards having apertures formed therein;

depositing solder in the apertures of the wiring boards;

stacking the wiring boards on top of one another and substantially in parallel; and

07-30-'04 14:15 FROM-Lerner & Greenberg

+9549251101

T-138 P06/10 U-605

Appl. No.: 10/090,289
Amdt. Dated July 30, 2004
Reply to Office action of May 3, 2004

melting the solder resulting in solder connections mechanically and electrically interconnecting the at least two stacked wiring boards, the solder connections extending through the apertures in at least one of the at least two stacked wiring boards and over one or more levels of the at least two stacked wiring boards.

Claim 16 (original): The method according to claim 15, which comprises providing the solder in the apertures in a form of solder balls having a smaller diameter than the apertures.

Claim 17 (original): The method according to claim 15, which comprises providing the solder in the apertures in a form of solder paste.

Claim 18 (previously presented): The method according to claim 15, which comprises fixing mechanically the wiring boards during the stacking step and before the melting step.

Claim 19 (original): The method according to claim 15, which comprises forming the semiconductor chips by the further steps of:

07-30-'04 14:15 FROM-Lerner & Greenberg

+9549251101

T-138 P07/10 U-605

Applic. No.: 10/090,289
Amdt. Dated July 30, 2004
Reply to Office action of May 3, 2004

stacking a number of semiconductor wafers one on top of another;

connecting contact vias with conductor tracks of the semiconductor wafers lying above or below; and

separating the semiconductor wafers into stacked semiconductor chips.

Claim 20 (original): The method according to claim 15, which comprises heating the solder to a soldering temperature for connecting the wiring boards.

Claim 21 (original): The method according to claim 15, wherein the apertures are provided near an edge of the at least two wiring boards.

Claim 22 (original): The method according to claim 15, further comprising applying supporting points to rear sides of the at least two wiring boards facing away from the semiconductor chips.

Claim 23 (cancelled).